

03/01/99
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Paul A. Farrar
Title: CONDUCTIVE STRUCTURES IN INTEGRATED CIRCUITS
Attorney Docket No.: 303.557US1

Jc618 U.S. PTO
09/25/94
03/01/99

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"Express Mail" mailing label number: EM287849297US Date of Deposit: March 1, 1999
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Conductive Structures in Integrated Circuits

Field of the Invention

5 This invention relates to integrated circuits, and more particularly, to
conductive structures used in integrated circuits.

Background of the Invention

10 As the dimensions of the devices and conductors that make up an integrated
circuit decrease, several problems arise. First, as the cross-sectional area of the
conductors decrease, the resistivity of the conductors increase, which, as current
flows in the conductors, results in an increase in the heat generated by the
conductors. Second, as the dimensions of the devices decrease, the devices and
conductors are packed more tightly in the integrated circuit, and the distance between
the conductors decreases, which results in an increase in the capacitance between the
15 conductors. This increase in capacitance reduces the speed at which information can
be transmitted along the conductors.

20 The first problem, increased heating resulting from a decrease in the cross-
sectional area of a conductor in an integrated circuit can cause the integrated circuit
to fail. Despite advances in devices, such as heat sinks which are designed to remove
heat from an integrated circuit, it is still important to reduce the heat generated
internal to the integrated circuit. Fabricating the conductors in an integrated circuit
from a metal, such as copper, which has a higher conductivity than the industry
standard aluminum conductor, is one way to eliminate the heat generated in the
conductor. Unfortunately, the use of copper as a conductor in an integrated circuit
25 generates another problem. Copper diffuses into the materials that make up the
integrated circuit, and the diffused copper alters the electrical properties of those
materials.

5 The second problem, increased capacitance between the conductors,
decreases the rate at which information can be transmitted along the conductors. One
approach to solving this problem is to use an insulator having a smaller dielectric
constant than the industry standard silicon dioxide, in order to decrease the
10 capacitance between the conductors. Polymers have a smaller dielectric constant
than silicon dioxide, but the use of polymers as insulators in integrated circuits
creates another problem. It is well known that both gold and copper are fast diffusers
in silicon, poisoning devices by degrading minority carrier lifetime. It is also known
that copper especially, diffuses rapidly through silicon oxide. It is also well known
15 that copper will react with organic acids like polyimide acid, which is used as a
precursor for the formation of many polyimide films, forming CuO which degrades
the resulting polymer. Therefore, a number of barrier materials have been studied to
prevent the penetration of copper into oxide or the reaction of copper with polymeric
acid precursors. Among the more successful are tantalum and tantalum nitride. It
20 has also been found that if polyimide is formed not from an acid but an ester based
starting material, that the reaction is reduced or eliminated, if the material is pure
enough. Therefore, if the polyimide is formed from an ester based precursor the
intermediate layer between the copper and the polymer acts mainly as an adhesion
layer assuring good adhesion between the resulting copper film and the polymer.
25 When a polymer is used in combination with aluminum conductors, the aluminum
does not affect the dielectric properties of the polymer; but the aluminum conductors
suffer from the previously described resistance-heating problem. To avoid this
problem, the thickness of the aluminum is increased. Unfortunately, increasing the
thickness of the aluminum increases the capacitance between the conductors.
Further, Aluminum has a high coefficient of thermal expansion which can result in
failures on the integrated circuit. For these and other reasons there is a need for the
present invention.

Summary of the Invention

The present invention solves many of the problems listed above and others which will become known to those skilled in the art upon reading and understanding the present disclosure. The invention includes a connector which is formed by a method comprising several processes. An insulator is deposited over a planarized surface, and a trench is etched in the insulator. A barrier layer is deposited on the insulator, and a seed layer is deposited on the barrier layer. The barrier layer and the seed layer are removed from selected areas or unused areas of the insulator, leaving the seed area, and a conductor is deposited on the seed area. Integrated circuits may be formed using the structure of the present invention having improved interconnect conductivity with lower capacitance.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of one embodiment of a connector embedded in an integrated circuit structure.

Figure 2A is a perspective view of a structure formed using a dual damascene process that is suitable for use in connection with the present invention.

Figure 2B is a cross-sectional view of a connective structure used in connection with a structure formed using a dual damascene process.

Figure 3 is a block diagram of a computer system suitable for use in connection with the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other

embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

5 In general, the present invention includes a connector conductor which is formed by a method comprising several alternative processes. In one embodiment, an insulator is deposited over a planarized surface, and a trench is etched in the insulator. A barrier layer is deposited on the insulator, and a seed layer is deposited on the barrier layer. The barrier layer and the seed layer are removed from selected areas of the insulator, leaving the seed area, and a conductor is deposited on the seed area by a selective deposition process. Many different embodiments of the present invention are described below. For example, In one other embodiment, the barrier layer is deposited on the insulator by physical vapor-deposition.

15 In other embodiments, the trench is etched to a depth about equal to the depth of the insulator. The barrier layer deposited on the Polyimide formed from a ester based monomer layer is selected from the group consisting of titanium, zirconium, and hafnium. The conductor may be selected from the group consisting of gold, silver, and copper, which may be deposited on the seed area by electroless plating. In yet other embodiments, the insulator deposited over the planarized surface is a polymer, the seed layer is copper and the barrier layer is tantalum nitride, and a layer of tantalum nitride is deposited above the conductor.

20 In another embodiment the barrier layer is deposited on a oxide layer and is selected from the group consisting of titanium, zirconium and hafnium; the conductor is aluminum or aluminum copper and the seed layer is aluminum, aluminum copper or copper.

25 In another embodiment, an oxide layer is deposited over a planarized surface, and a trench having a top is etched on the oxide layer. A barrier layer of tantalum or tantalum nitride is deposited on the oxide layer. A layer of copper is deposited on

the oxide layer. The barrier layer and the seed layer are removed from selected areas and unused areas of the oxide layer, leaving a seed area. A layer of copper is deposited on the seed area, and a layer of tantalum nitride is deposited above the copper layer.

5 In other embodiments, tantalum nitride is deposited to a depth of approximately one-hundred angstroms. The barrier layer of tantalum nitride is deposited by a non-anisotropic deposition technique. A connective structure may comprise an insulator deposited above a planarized surface. The insulator has a trench, and the trench has a trench surface. A barrier layer is above the trench
10 surface. A seed layer is above the barrier layer, and a conductor is above the seed layer.

 Figure 1 is a cross-sectional view of one embodiment of a connector embedded in an integrated circuit structure. Structure 100 comprises substrate 105, device 110, insulating layer 115, diffusion barrier layer 120, insulating layer 125,
15 trench 130, barrier layer 135, seed layer 140, conductor 145, and insulating layer 150.

 Device 110 is formed on substrate 105. Insulating layer 115 is deposited on substrate 105. Insulating layer 115 is planarized, and diffusion barrier layer 120 is deposited on planarized insulating layer 115. Insulating layer 125 is deposited on
20 diffusion barrier layer 120, and trench 130 is etched into insulating layer 125. Barrier layer 135 is deposited on insulating layer 125, and seed layer 140 is deposited on barrier layer 135. Seed layer 140 and barrier layer 135 are selectively removed from insulating layer 125, leaving seed area 155. Conductor 145 is deposited on seed area 155, and insulating layer 150 is deposited above insulating layer 125.

25 Substrate 105, in one embodiment, is silicon, however, the invention is not limited to a particular substrate material and the substrate material is not critical to the practice of the invention. Other substrate materials suitable for use in the present invention include germanium, gallium arsenide, and silicon-on-sapphire.

Device 110, in one embodiment, is an electronic device, such as a transistor, resistor, or capacitor, and is fabricated on substrate 105. The present invention is not limited to use in connecting any particular type of electronic device. Rather, the present invention is suitable for use in connecting a wide range of electronic devices.

5 For example, in one embodiment, the cross-sectional area of connector conductor 145 can be increased and then used to connect high current switching transistors.

Insulating layer 115, in one embodiment, blocks undesired current flow from substrate 105 to layers above insulating layer 115. The material selected for insulating layer 115 is not critical to the practice of the present invention. In one
10 embodiment, insulating layer 115 is silicon dioxide. After insulating layer 115 is deposited on substrate 105, the surface of insulating layer 115 is planarized. Chemical mechanical polishing or a similar process is suitable for planarizing the surface of insulating layer 115.

Diffusion barrier layer 120, in one embodiment, is deposited on insulating
15 layer 115 and blocks impurities from subsequent processing from entering insulating layer 115 and substrate 105. In one embodiment, a layer of Si_3N_4 is deposited on insulating layer 115 to form diffusion barrier layer 120.

Insulating layer 125 is deposited on diffusion barrier layer 120. In one
20 embodiment, insulating layer 125 is an oxide. In another embodiment, the oxide is silicon dioxide. In another embodiment, the oxide is a fluorinated silicon oxide. In another embodiment, insulating layer 125 is a polymer. In still another embodiment, the polymer is a foamed polymer. In still another embodiment, the polymer is a polyimide. The thickness of insulating layer 125, in one embodiment, is about equal to the thickness of connector conductor 145.

25 It is important to note that insulating layer 125 is deposited above a planarized surface, which in one embodiment is the planarized surface of insulating layer 115. Depositing insulating layer 125 above a planarized surface ensures that subsequent processes that remove seed layer 140 and barrier layer 135 from selected

areas or unused areas 160 of the surface of insulating layer 125 are performed on a planar surface, which makes the removal process fast and efficient. It also results in fewer defects to other integrated circuit structures during the removal process, when compared with a removal process performed on a non-planar surface.

5 Connector 165 is fabricated by etching trench 130 into insulating layer 125, depositing barrier layer 135 on insulating layer 125, depositing seed layer 140 on insulating layer 125, removing seed layer 140 and barrier layer 135 from selected areas 160 of insulating layer 125, and leaving seed area 155 at the bottom and along the sides of trench 130.

10 Trench 130 is etched to a depth and width that provide the desired resistance in connector 165. Since the resistance of conductor 145 is inversely proportional to the cross-sectional area of conductor 145, the greater the depth and width of trench 130, the less the resistance of conductor 145, for a given conductor. However, it is preferable to decrease the resistance of conductor 145 by increasing the width of
15 trench 130 as opposed to increasing the depth, since increasing the depth increases the capacitance between adjacent connectors, which limits the information transfer rate along conductor 145. Top 170 of trench 130 is in the same plane as the surface of insulating layer 125.

20 Barrier layer 135 is deposited on insulating layer 125 in order to block the flow of impurities, created during subsequent processing, into insulating layer 125. In one embodiment, barrier layer 135 is selected from the group consisting of titanium, zirconium, and hafnium. In another embodiment, the barrier layer is selected from the group consisting of zirconium and titanium. In still another embodiment, barrier layer 135 is tantalum nitride. In one embodiment, the thickness
25 of the barrier layer is between about fifty and about one-thousand angstroms. In one embodiment, the tantalum nitride is deposited to a depth of approximately one-hundred angstroms. The barrier layer is deposited by sputtering, physical vapor

deposition, or other vapor deposition technique. In one embodiment, a barrier layer 135 of tantalum nitride is deposited by a non-anisotropic deposition technique.

Seed layer 140 is deposited on barrier layer 135, in order to provide a site for depositing a metal to form a conducting integrated circuit connector. Seed layer 140 is formed from a conducting material. In one embodiment, seed layer 140 is selected from the group of conducting materials consisting of gold, silver, and copper. In another embodiment, seed layer 140 is an alloy of a metal selected from the group consisting of gold, silver, and copper. In still another embodiment, seed layer 140 is an aluminum-copper alloy. Seed layer 140 must be sufficiently thick to act as a seed layer for a selective deposition process. In one embodiment, a seed layer of copper is deposited to a depth of approximately five-hundred angstroms. In one embodiment, the seed layer is deposited by physical vapor deposition. In an alternate embodiment, the seed layer is deposited by chemical vapor-deposition.

Chemical mechanical polishing, in one embodiment, is used to remove barrier layer 135 and seed layer 140 from selected areas 160 of insulating layer 125. Seed layer 140 and barrier layer 135 are not removed from the seed area along the bottom and sides of trench 130. Since insulating layer 115 is planarized, only the surface of insulating layer 125, with the relatively thin barrier layer 135 and seed layer 140, are exposed to the chemical mechanical polishing process. A hard pad polish is preferred, in order to reduce the removal of seed layer 140 from trench 130. At the completion of the chemical mechanical polishing process, seed layer 140 remains on the bottom and sides of trench 130.

Conductor 145 is deposited on seed area 155, after barrier layer 135 and seed layer 140 are removed from selected areas 160 of insulating layer 125, leaving seed area 155. In one embodiment, conductor 145 is selected from the group consisting of gold, silver, and copper. In another embodiment, conductor 145 is an alloy of gold, silver, and copper. In still another embodiment, conductor 145 is an alloy of aluminum. Conductor 145, in one embodiment, is deposited by an electroless plating

process. In one embodiment, conductor 145 is deposited to a depth sufficient to fill trench 130.

Insulating layer 150, in one embodiment, is deposited above insulating layer 125, after barrier layer 135 and seed layer 140 are deposited on insulating layer 125, and conductor 145 is deposited on seed layer 140. In one embodiment, insulating layer 150 is silicon dioxide. In an alternate embodiment, insulating layer 150 is tantalum nitride. In a preferred embodiment, insulating layer 150 is tantalum nitride, barrier layer 135 is tantalum nitride, seed layer 140 is copper, and conductor 145 is copper. Device 110 can be connected to conductor 145 through conductive vias and other structures known in the art.

A specific use of the present invention is illustrated in Figure 2A and Figure 2B. Figure 2A shows a dual damascene structure suitable for use in connection with the present invention. Figure 2B shows the use of a dual damascene metallization process with a barrier layer of tantalum nitride and a copper conductor. However, the present invention is not meant to be limited to the use of a copper conductor and a tantalum nitride barrier layer. A variety of materials, such as aluminum, aluminum-copper, and gold can be used in connection with the present invention and the dual damascene process. In addition, a variety of devices, such as memory cells, capacitors, and transistors, can be interconnected using such a dual damascene process with a copper, gold, silver, aluminum or aluminum-copper material as an interconnect.

As illustrated in Figure 2A, substrate 203 is conventionally processed using a dual damascene process up to the point where the first level of interconnection metal is to be formed. The conventional processing includes etching oxide 206 to form trench 209, forming a photoresist pattern to define contact site 212, and then etching oxide 206 to form contact site 212. The photoresist is removed to leave a finished damascene structure.

Also illustrated in Figure 2A, contact site 212 is defined to device 215 of substrate 203. The damascene structure has two levels, a contact level at device 215 underlying a metallization level. At the metallization level, trench 209 is defined and extends over contact site 212 and defines the position and width of the metal line that is subsequently formed in trench 209 and contact site 212.

To form contact site 212 and trench 209, the structure illustrated in Figure 2A is patterned using conventional photolithography and etching. Due to the nature of the dual damascene process, the depth of the etch is variable across the surface of the substrate, e.g., the etch depth is greater where contact site 212 is defined and less where only trench 209 is defined. Thus, two mask and etch steps can be utilized in a conventional photolithographic process to define the contact site 212 separately from the trench 209. Alternatively, a gray mask pattern can be utilized to define contact site 212 and trench 209 simultaneously in one photolithographic mask and etch step.

Figure 2B is a cross-sectional view of trench 209 and contact site 212 of Figure 2A. After trench 209 and contact site 212 are formed, a barrier layer of tantalum nitride 221 is deposited above the trench surface. Next, a seed layer of copper 224 is deposited above the barrier layer. Next, a layer of copper 227 is deposited above seed layer 224. Still referring to Figure 2B, copper 218 is deposited and etched back in the contact site 212 and trench 209. Alternatively, gold, aluminum, silver, or an aluminum-copper composite can be deposited in trench 209 and contact site 212. A wide variety of suitable methods are available for depositing copper 218. Most techniques are physical techniques (e.g., sputtering and evaporating). The advantage of a dual damascene process is that only one copper 218 deposition step is needed to fill both contact site 212 and trench 209. Excess metal 218 deposited outside of the defined contact site 212 and trench 209 is etched back using any suitable method. For example, planarization (e.g., using at least one of a chemical or mechanical technique) is one suitable method. The sequence of

steps described is then repeated, if necessary, depending on the number of conductive layers in the metallization level of the substrate.

Referring to Figure 3, a block diagram of a system level embodiment of the present invention is shown. System 300 comprises processor 305 and memory device 310, which includes conductive structures of one or more of the types described above in conjunction with Figure 1, Figure 2A, and Figure 2B. Memory device 310 comprises memory array 315, address circuitry 320, and read circuitry 330, and is coupled to processor 305 by address bus 335, data bus 340, and control bus 345. Processor 305, through address bus 335, data bus 340, and control bus 345 communicates with memory device 310. In a read operation initiated by processor 305, address information, data information, and control information are provided to memory device 310 through busses 335, 340, and 345. This information is decoded by addressing circuitry 320, including a row decoder and a column decoder, and read circuitry 330. Successful completion of the read operation results in information from memory array 315 being communicated to processor 305 over data bus 340.

Conclusion

Several embodiments of a method for fabricating conducting structures in an integrated circuit have been described. These embodiments exhibit reduced resistance induced heating in the conducting structures and low capacitive coupling between conductors. Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A method of forming a conductor comprising:
depositing an insulator over a planarized surface;
5 etching a trench having a depth on the insulator;
depositing a barrier layer on the insulator;
depositing a seed layer on the barrier layer;
removing the barrier layer and seed layer from selected areas of the insulator,
leaving a seed area; and
10 depositing a conductor on the seed area by a selective deposition process.
2. The method of claim 1, wherein depositing the barrier layer on the insulator
comprises:
depositing the barrier layer on the insulator by physical vapor-deposition.
15
3. The method of claim 1, wherein etching a trench on the insulator comprises:
etching the trench to a depth of about equal to the depth of the insulator.
4. A method of forming a conductor comprising:
20 depositing an oxide layer over a planarized surface;
etching a trench on the oxide layer;
depositing a barrier layer on the oxide layer;
depositing a seed layer on the barrier layer;
removing the barrier layer and seed layer from unused areas of the oxide
25 layer, leaving a seed area; and
depositing a conductor on the seed area.

5. The method of claim 4, wherein depositing an oxide layer over a planarized surface comprises:

depositing a silicon dioxide layer over the planarized surface.

5 6. The method of claim 4, wherein depositing an oxide layer over a planarized surface comprises:

depositing a fluorinated silicon oxide layer over the planarized surface.

10 7. The method of claim 4, wherein depositing a seed layer on the barrier layer comprises:

depositing the seed layer on the barrier layer by physical vapor-deposition.

8. A method of forming a conductor comprising:

depositing a polymer layer over a planarized surface;

15 etching a trench on the polymer layer;

depositing a barrier layer on the polymer layer;

depositing a seed layer on the polymer layer;

removing the seed layer from selected areas of the polymer layer, leaving a seed area; and

20 depositing a conductor on the seed area.

9. The method of claim 8, wherein depositing a polymer layer over a planarized surface comprises:

depositing a polyimide layer over the planarized surface.

25

10. The method of claim 8, wherein depositing a polymer layer over a planarized surface comprises:

depositing a foamed polymer layer over the planarized surface.

11. The method of claim 8, wherein depositing a seed layer on the polymer layer comprises:

depositing the seed layer on the polymer by physical vapor-deposition.

5 12. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer tantalum on the oxide layer;

depositing a seed layer selected from the group consisting of gold, silver, and

10 copper on the oxide layer;

removing the barrier layer and seed layer from unused areas of the oxide

layer, leaving a seed area; and

depositing a conductor on the seed area.

15 13. The method of claim 12, wherein depositing a barrier layer tantalum on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

20 14. The method of claim 12, wherein depositing the barrier layer of tantalum and gold on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

25 15. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

depositing a barrier layer tantalum on the oxide layer;

depositing a seed layer of gold on the oxide layer;

removing the barrier layer and seed layer from selected areas of the oxide layer, leaving a seed area; and
depositing gold on the seed area.

5 16. The method of claim 15, wherein depositing a barrier layer tantalum on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

10 17. The method of claim 15, wherein depositing the barrier layer of tantalum and gold on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

15 18. The method of claim 15, wherein depositing gold on the seed area comprises:
depositing gold on the seed area by electroless plating.

19. A method of forming a conductor comprising:
depositing an oxide layer over a planarized surface;
etching a trench on the oxide layer;
20 depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer;
depositing a seed layer of silver on the oxide layer;
removing the barrier layer and seed layer from selected areas of the oxide layer, leaving a seed area; and
25 depositing silver on the seed area.

20. The method of claim 19, wherein depositing the barrier layer of titanium and silver on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

21. The method of claim 19, wherein depositing a seed layer of titanium and silver on the oxide layer comprises:

5 depositing the seed layer of titanium and silver to a depth of between fifty angstroms and two-thousand angstroms.

22. The method of claim 19, wherein depositing silver on the seed area comprises:

10 depositing silver on the seed area by electroless plating.

23. A method of forming a conductor comprising:

depositing an oxide layer over a planarized surface;

etching a trench on the oxide layer;

15 depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer; depositing a seed layer of copper on the oxide layer; removing the barrier layer and seed layer from selected areas or unused areas of the oxide layer, leaving a seed area; and

20 depositing aluminum on the seed area.

24. The method of claim 23, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:

25 depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

25. The method of claim 23, wherein depositing the barrier layer of titanium and aluminum on the oxide layer comprises:

depositing the barrier layer by physical vapor-deposition.

26. The method of claim 23, wherein depositing copper on the seed area comprises:

5 depositing aluminum on the seed area by selective chemical vapor-deposition (CVD).

27. A method of forming a conductor comprising:

depositing a polymer layer over a planarized surface;

10 etching a trench on the polymer layer;

depositing a barrier layer selected from the group consisting of titanium,

zirconium, and hafnium on the polymer layer;

depositing a seed layer selected from the group consisting of gold, silver, and copper on the polymer layer;

15 removing the barrier layer and seed layer from selected areas of the polymer layer, leaving a seed area; and

depositing a conductor on the seed area.

28. The method of claim 27, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

29. The method of claim 27, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:

depositing the barrier layer by physical vapor-deposition.

30. A method of forming a conductor comprising:
depositing a polymer layer over a planarized surface;
etching a trench on the polymer layer;
depositing a barrier layer selected from the group consisting of titanium,
5 zirconium, and hafnium on the polymer layer;
depositing a seed layer of gold on the polymer layer;
removing the barrier layer and seed layer from selected areas or unused areas
of the polymer layer, leaving a seed area; and
depositing gold on the seed area.

10

31. The method of claim 30, wherein depositing a barrier layer selected from the
group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:
depositing the barrier layer to a depth of between fifty angstroms and one-
thousand angstroms.

15

32. The method of claim 30, wherein depositing a barrier layer selected from the
group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:
depositing the barrier layer by physical vapor-deposition.

20

33. The method of claim 30, wherein depositing gold on the seed area comprises:
depositing gold on the seed area by electroless plating.

25

34. A method of forming a conductor comprising:
depositing a polymer layer over a planarized surface;
etching a trench on the polymer layer;
depositing a barrier layer selected from the group consisting of titanium,
zirconium, and hafnium on the polymer layer;
depositing a seed layer of silver on the polymer layer;

removing the barrier layer and seed layer from selected areas of the polymer layer, leaving a seed area; and
depositing silver on the seed area.

5 35. The method of claim 34, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the oxide layer comprises:
depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

10 36. The method of claim 34, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:
depositing the barrier layer by physical vapor-deposition.

15 37. The method of claim 34, wherein depositing silver on the seed area comprises:
depositing silver on the seed area by electroless plating.

20 38. A method of forming a conductor comprising:
depositing a polymer layer over a planarized surface;
etching a trench on the polymer layer;
depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer;
depositing a seed layer of copper on the polymer layer;
25 removing the barrier layer and seed layer from unused areas of the polymer layer, leaving a seed area; and
depositing copper on the seed area.

39. The method of claim 38, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:

5 depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

40. The method of claim 38, wherein depositing a barrier layer selected from the group consisting of titanium, zirconium, and hafnium on the polymer layer comprises:

10 depositing the barrier layer by physical vapor-deposition.

41. The method of claim 38, wherein depositing copper on the seed area comprises:

15 depositing copper on the seed area by electroless plating.

42. A method of forming a conductor comprising:

20 depositing an oxide layer over a planarized surface;
etching a trench on the oxide layer;
depositing a barrier layer selected from the group consisting of zirconium and titanium on the oxide layer;
depositing a seed layer of aluminum-copper on the oxide layer;
removing the barrier layer and seed layer from selected areas of the oxide layer, leaving a seed area; and
depositing a conductor on the seed area.

25 43. The method of claim 42, wherein depositing a barrier layer selected from the group consisting of zirconium and titanium on the oxide layer comprises:

depositing the barrier layer to a depth of between fifty angstroms and one-thousand angstroms.

44. The method of claim 42, wherein depositing the barrier layer selected from
5 the group consisting of zirconium and titanium on the oxide layer comprises:
depositing the barrier layer by physical vapor-deposition.

45. A method of forming a conductor comprising:
depositing an oxide layer over a planarized surface;
10 etching a trench on the oxide layer;
depositing a barrier layer of zirconium on the oxide layer;
depositing a seed layer of aluminum-copper on the oxide layer;
removing the barrier layer and seed layer from selected areas of the oxide
layer, leaving a seed area; and
15 depositing aluminum on the seed area.

46. The method of claim 45, wherein depositing a barrier layer of zirconium on
the oxide layer comprises:
20 depositing the barrier layer to a depth of between fifty angstroms and one-
thousand angstroms.

47. The method of claim 45, wherein depositing a barrier layer of zirconium on
the oxide layer comprises:
25 depositing the barrier layer by physical vapor-deposition.

48. The method of claim 45, wherein depositing aluminum on the seed area
comprises:
depositing aluminum on the seed area by chemical vapor-deposition.

49. The method of claim 45, wherein depositing aluminum on the seed area comprises:

depositing an amount of aluminum sufficient to fill the trench.

5 50. A method of forming a conductor comprising:
depositing an oxide layer over a planarized surface;
etching a trench on the oxide layer;
depositing a barrier layer of titanium on the oxide layer;
depositing a seed layer of aluminum-copper on the oxide layer;
10 removing the barrier layer and seed layer from selected areas or unused areas
of the oxide layer, leaving a seed area; and
depositing aluminum on the seed area.

15 51. The method of claim 50, wherein depositing a barrier layer of titanium on the
oxide layer comprises:
depositing the barrier layer to a depth of between fifty angstroms and one-
thousand angstroms.

20 52. The method of claim 50, wherein depositing a barrier layer of titanium on the
oxide layer comprises:
depositing the barrier layer by physical vapor-deposition.

25 53. The method of claim 50, wherein depositing aluminum on the seed area
comprises:
depositing aluminum on the seed area by chemical vapor-deposition.

54. The method of claim 50, wherein depositing a seed layer of titanium on the
oxide layer comprises:

depositing the seed layer of titanium on the oxide layer by chemical vapor-deposition.

55. The method of claim 50, wherein depositing aluminum on the seed area
5 comprises:

depositing an amount of aluminum sufficient to fill the trench.

56. A method of forming a conductor comprising:
depositing an oxide layer over a planarized surface;
10 etching a trench having a top on the oxide layer;
depositing a barrier layer of tantalum nitride on the oxide layer;
depositing a seed layer of copper on the tantalum nitride layer;
removing the barrier layer and seed layer from selected areas of the oxide
layer;
15 depositing a conductor on the seed area leaving a seed area; and
depositing a layer of tantalum nitride above the conductor.

57. The method of claim 56, wherein depositing a barrier layer of tantalum
nitride on the oxide layer comprises:

20 depositing approximately one-hundred angstroms of tantalum nitride.

58. The method of claim 56, wherein depositing a seed layer of copper on the
tantalum nitride layer comprises:

25 depositing approximately five-hundred angstroms of copper on the tantalum
nitride layer.

59. The method of claim 56, wherein depositing a barrier layer of tantalum
nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride by a non-anisotropic deposition technique.

60. The method of claim 56, wherein depositing a seed layer of copper on the
5 barrier layer of tantalum nitride comprises:

depositing the seed layer of copper on the tantalum nitride layer by a non-anisotropic deposition technique.

61. The method of claim 56, wherein depositing a barrier layer of tantalum
10 nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride to a depth of between fifty angstroms and one-thousand angstroms.

62. The method of claim 56, wherein depositing a barrier layer of tantalum
15 nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride on the oxide layer by chemical vapor-deposition.

63. The method of claim 56, wherein depositing a seed layer of copper on the
20 layer of tantalum nitride comprises:

depositing the seed layer copper on the barrier layer to a depth of approximately five-hundred angstroms below the top of the trench.

64. The method of claim 56, wherein depositing a barrier layer of tantalum
25 nitride above the conductor comprises:

depositing the barrier layer of tantalum nitride above the conductor to a depth of approximate five-hundred angstroms.

65. The method of claim 56, wherein depositing an oxide layer over a planarized surface comprises:

depositing a silicon dioxide layer over the planarized surface.

5 66. The method of claim 56, wherein depositing an oxide layer over a planarized surface comprises:

depositing a fluorinated silicon oxide layer over the planarized surface.

67. A method of forming a conductor comprising:

10 depositing an oxide layer over a planarized surface;

etching a trench having a top on the oxide layer;

depositing a barrier layer of tantalum nitride on the oxide layer;

depositing a seed layer of copper on the oxide layer;

removing the barrier layer and seed layer from selected areas of the oxide

15 layer, leaving a seed area;

depositing a layer of copper on the seed area; and

depositing a layer of tantalum nitride above the layer of copper.

68. The method of claim 67, wherein depositing a barrier layer of tantalum
20 nitride on the oxide layer comprises:

depositing approximately one-hundred angstroms of tantalum nitride.

69. The method of claim 67, wherein depositing a seed layer of copper on the oxide layer comprises:

25 depositing approximately five-hundred angstroms of copper on the oxide layer.

70. The method of claim 67, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride by a non-anisotropic deposition technique.

5

71. The method of claim 67, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride to a depth of between fifty angstroms and one-thousand angstroms.

10

72. The method of claim 67, wherein depositing a barrier layer of tantalum nitride on the oxide layer comprises:

depositing the barrier layer of tantalum nitride on the oxide layer by chemical vapor-deposition.

15

73. The method of claim 67, wherein depositing a layer of copper on the seed area comprises:

depositing the layer of copper on the seed area by chemical vapor-deposition.

20

74. The method of claim 67, wherein depositing a layer of copper on the seed area comprises:

depositing the layer of copper on the seed area to a depth of approximately five-hundred angstroms below the top of the trench.

25

75. The method of claim 67, wherein depositing a layer of tantalum nitride above the copper comprises:

depositing the layer of tantalum nitride above the copper to a depth of approximate five-hundred angstroms.

76. The method of claim 67, wherein depositing an oxide layer over a planarized surface comprises:

depositing a silicon dioxide layer over the planarized surface.

5 77. The method of claim 67, wherein depositing an oxide layer over a planarized surface comprises:

depositing a fluorinated silicon oxide layer over the planarized surface.

10 78. A connective structure comprising:
an insulator above a planarized surface, the insulator having a trench, the
trench having a trench surface;
a barrier layer above the trench surface;
a seed layer above the barrier layer; and
a conductor above the seed layer.

15 79. The connective structure of claim 78, wherein the insulator has a depth, the trench has a depth and the depth of the trench is about equal to the depth of the insulator.

20 80. A connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer above the trench surface;
a seed layer above the barrier layer; and
25 a conductor above the seed layer.

81. The connective structure of claim 80, wherein the oxide layer is a silicon dioxide layer.

82. The connective structure of claim 80, wherein the oxide layer is a fluorinated silicon oxide layer.

5 83. A connective structure comprising:
a polymer layer above the planarized surface, the polymer layer having a
trench, the trench having a trench surface;
a barrier layer above the trench surface;
a seed layer above the barrier layer; and
10 a conductor above the seed layer.

84. The connective structure of claim 83, wherein the polymer layer is a polyimide layer.

15 85. The connective structure of claim 83, wherein the polymer layer is a foamed polymer layer.

20 86. A connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer tantalum above the trench surface;
a seed layer selected from the group consisting of gold, silver, and copper
above the barrier layer; and
a conductor above the seed layer.

25 87. The connective structure of claim 86, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

88. A connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer tantalum above the trench surface;
a seed layer of gold above the barrier layer; and
a gold layer above the seed layer.

89. The connective structure of claim 88, wherein the barrier layer has a depth of
between fifty angstroms and one-thousand angstroms.

90. A connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer tantalum above the trench surface; and
a gold layer above the barrier layer.

91. A connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer tantalum above the trench surface;
a seed layer of silver above the barrier layer; and
a silver layer above the barrier layer.

92. The connective structure of claim 91, wherein the barrier layer has a depth of
between fifty angstroms and one-thousand angstroms.

93. A connective structure comprising:

an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer tantalum above the trench surface; and
a silver layer above the barrier layer.

5

94. A connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer tantalum above the trench surface;
10 a seed layer of copper above the barrier layer; and
a copper layer above the seed layer.

95. The connective structure of claim 94, wherein the barrier layer has a depth of
between fifty angstroms and one-thousand angstroms.

15

96. A connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench,
the trench having a trench surface;
a barrier layer tantalum above the trench surface; and
20 a copper layer above the barrier layer.

20

97. A connective structure comprising:
a polymer layer above a planarized surface, the polymer layer having a
trench, the trench having a trench surface;
25 a barrier layer selected from the group consisting of titanium, zirconium, and
hafnium above the trench surface;
a seed layer selected from the group consisting of gold, silver, and copper
above the barrier layer; and

25

a conductor layer above the seed layer.

98. The connective structure of claim 97, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

5

99. A connective structure comprising:
a polymer layer above a planarized surface, the polymer layer having a
trench, the trench having a trench surface;
a barrier layer selected from the group consisting of titanium, zirconium, and
hafnium above the trench surface;
a seed layer of gold above the barrier layer; and
a gold layer above the seed layer.

10

100. The connective structure of claim 99, wherein the barrier layer has a depth of between fifty and one-thousand angstroms.

15

101. A connective structure comprising:
a polymer layer above a planarized surface, the polymer layer having a
trench, the trench having a trench surface;
a barrier layer selected from the group consisting of titanium, zirconium, and
hafnium above the trench surface; and
a gold layer above the barrier layer.

20

102. A connective structure comprising:
a polymer layer above a planarized surface, the polymer layer having a
trench, the trench having a trench surface;
a barrier layer selected from the group consisting of titanium, zirconium, and
hafnium above the trench surface;

25

a seed layer of silver above the barrier layer; and
a silver layer above the seed layer.

103. The connective structure of claim 102, wherein the barrier layer has a depth
5 of between fifty angstroms and one-thousand angstroms.

104. A connective structure comprising:
a polymer layer above a planarized surface, the polymer layer having a
trench, the trench having a trench surface;
10 a barrier layer selected from the group consisting of titanium, zirconium, and
hafnium above the trench surface; and
a silver layer above the barrier layer.

105. A connective structure comprising:
15 a polymer layer above a planarized surface, the polymer layer having a
trench, the trench having a trench surface;
a barrier layer selected from the group consisting of titanium, zirconium, and
hafnium above the trench surface;
a seed layer of copper above the barrier layer; and
20 a copper layer above the seed layer.

106. The connective structure of claim 105, wherein the barrier layer has a depth
of between fifty angstroms and one-thousand angstroms.

25 107. A connective structure comprising:
a polymer layer above a planarized surface, the polymer layer having a
trench, the trench having a trench surface;

a barrier layer selected from the group consisting of titanium, zirconium, and hafnium above the trench surface;
a seed layer of copper above the barrier layer; and
a copper layer above the seed layer.

5

108. A connective structure comprising:
an oxide layer above a planarized surface, the oxide layer having a trench, the trench having a trench surface;
a barrier layer selected from the group consisting of zirconium and titanium
10 above the trench surface;
a seed layer of aluminum-copper above the barrier layer; and
a conductor above the seed layer.

109. The connective structure of claim 108, wherein the barrier layer has a depth
15 of between fifty angstroms and one-thousand angstroms.

110. A connective structure comprising:
an oxide layer above a planarized surface, the oxide layer having a trench, the trench having a trench surface;
20 a barrier layer selected of zirconium above the trench surface;
a seed layer of aluminum-copper above the barrier layer; and
an aluminum layer above the seed layer.

111. The connective structure of claim 110, wherein the barrier layer has a depth
25 of between fifty and one-thousand angstroms.

112. The connective structure of claim 110, wherein the aluminum layer fills the trench.

113. A connective structure comprising:
an oxide layer above a planarized surface, the oxide layer having a trench, the
trench having a trench surface;
a barrier layer of titanium above the trench surface;
5 a seed layer of aluminum-copper above the barrier layer; and
an aluminum layer above the seed layer.

114. The connective structure of claim 113, wherein the barrier layer has a depth o
between fifty angstroms and one-thousand angstroms.

115. The connective structure of claim 113, where the aluminum layer fills the
trench.

116. A connective structure comprising:
15 an oxide layer above a planarized surface, the oxide layer having a trench, the
trench having a trench surface;
a barrier layer of tantalum nitride above the trench surface;
a seed layer of copper above the barrier layer;
an conductor layer above the seed layer; and
20 a tantalum nitride layer above the conductor layer.

117. The connective structure of claim 116, wherein the depth of the barrier layer
is approximately one-hundred angstroms.

25 118. The connective structure of claim 116, wherein the seed layer is
approximately five-hundred angstroms of copper.

119. The connective structure of claim 116, wherein the barrier layer is between fifty angstroms and one-thousand angstroms.

120. The connective structure of claim 116, wherein the trench has a top and the seed layer is approximately five-hundred angstroms below the top of the trench.

121. The connective structure of claim 116, wherein the barrier layer has a depth of approximately five-hundred angstroms.

122. The connective structure of claim 116, wherein the oxide layer is a silicon dioxide layer.

123. The connective structure of claim 116, wherein the oxide layer is a fluorinated silicon oxide layer.

124. A connective structure comprising:
an oxide layer above a planarized surface, the oxide layer having a trench, the trench having a trench surface;
a barrier layer of tantalum nitride above the trench surface;
a seed layer of copper above the barrier layer;
a copper layer above the seed layer; and
a tantalum nitride layer above the copper layer.

125. The connective structure of claim 124, wherein the barrier layer has a depth of approximately one-hundred angstroms.

126. The connective structure of claim 124, wherein the seed layer has a depth of approximately five-hundred angstroms.

127. The connective structure of claim 124, wherein the barrier layer has a depth of between approximately fifty angstroms and one-thousand angstroms.

5 128. The connective structure of claim 124, wherein the trench has a top and the copper is approximately five-hundred angstroms below the top of the trench.

129. The connective structure of claim 124, wherein the tantalum nitride above the copper is deposited to a depth of approximately five-hundred angstroms.

10 130. The connective structure of claim 124, wherein the oxide layer is a silicon dioxide layer.

131. The connective structure of claim 124, wherein the oxide layer is a fluorinated silicon oxide layer.

15

132. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure

20

comprising:

an insulator above a planarized surface, the insulator having a trench,

the trench having a trench surface;

a barrier layer above the trench surface;

a seed layer above the barrier layer; and

25

a conductor above the seed layer.

133. The computer system of claim 132, wherein the insulator has a depth, the trench has a depth and the depth of the trench is about equal to the depth of the insulator.

5 134. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

10 an oxide layer above the planarized surface, the oxide layer having a trench, the trench having a trench surface;

a barrier layer above the trench surface;

a seed layer above the barrier layer; and

a conductor above the seed layer.

15

135. The computer system of claim 134, wherein the oxide layer is a silicon dioxide layer.

20

136. The computer system of claim 134, wherein the oxide layer is a fluorinated silicon oxide layer.

25

137. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a polymer layer above the planarized surface, the polymer layer having a trench, the trench having a trench surface;

a barrier layer above the trench surface;
a seed layer above the barrier layer; and
a conductor above the seed layer.

5 138. The computer system of claim 137, wherein the polymer layer is a polyimide layer.

139. The computer system of claim 137, wherein the polymer layer is a foamed polymer layer.

10

140. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure

15

comprising:

an oxide layer above the planarized surface, the oxide layer having a
trench, the trench having a trench surface;

a barrier layer tantalum above the trench surface;

a seed layer selected from the group consisting of gold, silver, and

20

copper above the barrier layer; and

a conductor above the seed layer.

141. The computer system of claim 140, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

25

142. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

an oxide layer above the planarized surface, the oxide layer having a trench, the trench having a trench surface;
a barrier layer tantalum above the trench surface;
a seed layer of gold above the barrier layer; and
a gold layer above the seed layer.

143. The computer system of claim 142, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

144. A computer system comprising:
a processor;
a device coupled to the processor; and
a connective structure coupled to the device, the connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench, the trench having a trench surface;
a barrier layer tantalum above the trench surface; and
a gold layer above the barrier layer.

145. A computer system comprising:
a processor;
a device coupled to the processor; and
a connective structure coupled to the device, and the connective structure comprising:
an oxide layer above the planarized surface, the oxide layer having a trench, the trench having a trench surface;

a barrier layer tantalum above the trench surface;
a seed layer of silver above the barrier layer; and
a silver layer above the barrier layer.

5 146. The computer system of claim 145, wherein the barrier layer has a depth of
between fifty angstroms and one-thousand angstroms.

10 147. A computer system comprising:
a processor;
a device coupled to the processor; and
a connective structure coupled to the device, the connective structure
comprising:
an oxide layer above the planarized surface, the oxide layer having a
trench, the trench having a trench surface;
15 a barrier layer tantalum above the trench surface; and
a silver layer above the barrier layer.

20 148. A computer system comprising:
a processor;
a device coupled to the processor; and
a connective structure coupled to the device, the connective structure
comprising:
an oxide layer above the planarized surface, the oxide layer having a
trench, the trench having a trench surface;
25 a barrier layer tantalum above the trench surface;
a seed layer of copper above the barrier layer; and
a copper layer above the seed layer.

149. The computer system of claim 148, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

150. A computer system comprising:

5

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

10

an oxide layer above the planarized surface, the oxide layer having a trench, the trench having a trench surface;

a barrier layer tantalum above the trench surface; and

a copper layer above the barrier layer.

151. A computer system comprising:

15

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

20

a polymer layer above a planarized surface, the polymer layer having a trench, the trench having a trench surface;

a barrier layer tantalum above the trench surface;

a seed layer selected from the group consisting of gold, silver, and copper above the barrier layer; and

a conductor layer above the seed layer.

25

152. The computer system of claim 151, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

153. A computer system comprising:
a processor;
a device coupled to the processor; and
a connective structure coupled to the device, the connective structure
5 comprising:
a polymer layer above a planarized surface, the polymer layer having
a trench, the trench having a trench surface;
a barrier layer selected from the group consisting of titanium,
zirconium, and hafnium above the trench surface;
10 a seed layer of gold above the barrier layer; and
a gold layer above the seed layer.

154. The computer system of claim 153, wherein the barrier layer has a depth of
between fifty and one-thousand angstroms.

155. A computer system comprising:
a processor;
a device coupled to the processor; and
a connective structure coupled to the device, and the connective structure
20 comprising:
a polymer layer above a planarized surface, the polymer layer having
a trench, the trench having a trench surface;
a barrier layer selected from the group consisting of titanium,
zirconium, and hafnium above the trench surface; and
25 a gold layer above the barrier layer.

156. A computer system comprising:
a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a polymer layer above a planarized surface, the polymer layer having

5 a trench, the trench having a trench surface;

a barrier layer selected from the group consisting of titanium,
zirconium, and hafnium above the trench surface;

a seed layer of silver above the barrier layer; and

a silver layer above the seed layer.

10

157. The computer system of claim 156, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

158. A computer system comprising:

15 a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a polymer layer above a planarized surface, the polymer layer having

20 a trench, the trench having a trench surface;

a barrier layer selected from the group consisting of titanium,
zirconium, and hafnium above the trench surface; and

a silver layer above the barrier layer.

25 159. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a polymer layer above a planarized surface, the polymer layer having a trench, the trench having a trench surface;
a barrier layer selected from the group consisting of titanium, zirconium, and hafnium above the trench surface;
a seed layer of copper above the barrier layer; and
a copper layer above the seed layer.

10 160. The computer system of claim 159, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

161. A computer system comprising:

a processor;

15 a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

a polymer layer above a planarized surface, the polymer layer having a trench, the trench having a trench surface;

20 a barrier layer selected from the group consisting of titanium, zirconium, and hafnium above the trench surface;

a seed layer of copper above the barrier layer; and

a copper layer above the seed layer.

25 162. A computer system comprising:

a processor;

a device coupled to the processor; and

a connective structure coupled to the device, the connective structure comprising:

an oxide layer above a planarized surface, the oxide layer having a trench, the trench having a trench surface;

5 a barrier layer selected from the group consisting of zirconium and titanium above the trench surface;

a seed layer of aluminum-copper above the barrier layer; and
a conductor above the seed layer.

10 163. The computer system of claim 162, wherein the barrier layer has a depth of between fifty angstroms and one-thousand angstroms.

164. A computer system comprising:

a processor;

15 a device coupled to the processor; and

a connective structure coupled to the device, and the connective structure comprising:

an oxide layer above a planarized surface, the oxide layer having a trench, the trench having a trench surface;

20 a barrier layer selected of zirconium above the trench surface;

a seed layer of aluminum-copper above the barrier layer; and

an aluminum layer above the seed layer.

25 165. The computer system of claim 164, wherein the barrier layer has a depth of between fifty and one-thousand angstroms.

166. The computer system of claim 164, wherein the aluminum layer fills the trench.

167. A computer system comprising:
a processor;
a device coupled to the processor; and
a connective structure coupled to the device, the connective structure
5 comprising:
an oxide layer above a planarized surface, the oxide layer having a
trench, the trench having a trench surface;
a barrier layer of titanium above the trench surface;
a seed layer of aluminum-copper above the barrier layer; and
10 an aluminum layer above the seed layer.
168. The computer system of claim 167, wherein the barrier layer has a depth o
between fifty angstroms and one-thousand angstroms.
- 15 169. The computer system of claim 167, where the aluminum layer fills the trench.
170. A computer system comprising:
a processor;
a device coupled to the processor; and
20 a connective structure coupled to the device, the connective structure
comprising:
an oxide layer above a planarized surface, the oxide layer having a
trench, the trench having a trench surface;
a barrier layer of tantalum nitride above the trench surface;
25 a seed layer of copper above the barrier layer;
an conductor layer above the seed layer; and
a tantalum nitride layer above the conductor layer.

171. The computer system of claim 170, wherein the depth of the barrier layer is approximately one-hundred angstroms.

5 172. The computer system of claim 170, wherein the seed layer is approximately five-hundred angstroms of copper.

173. The computer system of claim 170, wherein the barrier layer is between fifty angstroms and one-thousand angstroms.

10 174. The computer system of claim 170, wherein the trench has a top and the seed layer is approximately five-hundred angstroms below the top of the trench.

15 175. The computer system of claim 170, wherein the barrier layer has a depth of approximately five-hundred angstroms.

176. The computer system of claim 170, wherein the oxide layer is a silicon dioxide layer.

20 177. The computer system of claim 170, wherein the oxide layer is a fluorinated silicon oxide layer.

178. A computer system comprising:
a processor;
a device coupled to the processor; and
25 a connective structure coupled to the device, the connective structure comprising:
an oxide layer above a planarized surface, the oxide layer having a
trench, the trench having a trench surface;

a barrier layer of tantalum nitride above the trench surface;
a seed layer of copper above the barrier layer;
a copper layer above the seed layer; and
a tantalum nitride layer above the copper layer.

5

179. The computer system of claim 178, wherein the barrier layer has a depth of approximately one-hundred angstroms.

10

180. The computer system of claim 178, wherein the seed layer has a depth of approximately five-hundred angstroms.

181. The computer system of claim 178, wherein the barrier layer has a depth of between approximately fifty angstroms and one-thousand angstroms.

15

182. The computer system of claim 178, wherein the trench has a top and the copper is approximately five-hundred angstroms below the top of the trench.

183. The computer system of claim 178, wherein the tantalum nitride above the copper is deposited to a depth of approximately five-hundred angstroms.

20

184. The computer system of claim 178, wherein the oxide layer is a silicon dioxide layer.

25

185. The computer system of claim 178, wherein the oxide layer is a fluorinated silicon oxide layer.

Abstract of the Disclosure

A connective structure is formed by first depositing an insulator over a planarized surface. A trench is etched in the insulator. A barrier layer is deposited on the insulator. A seed layer is deposited on the barrier layer. The barrier layer and seed layer are selectively removed from areas of the insulator leaving an exposed seed area. A conductor is deposited on the exposed seed area. As many of these connective structures as desired may be stacked in an integrated circuit structure.

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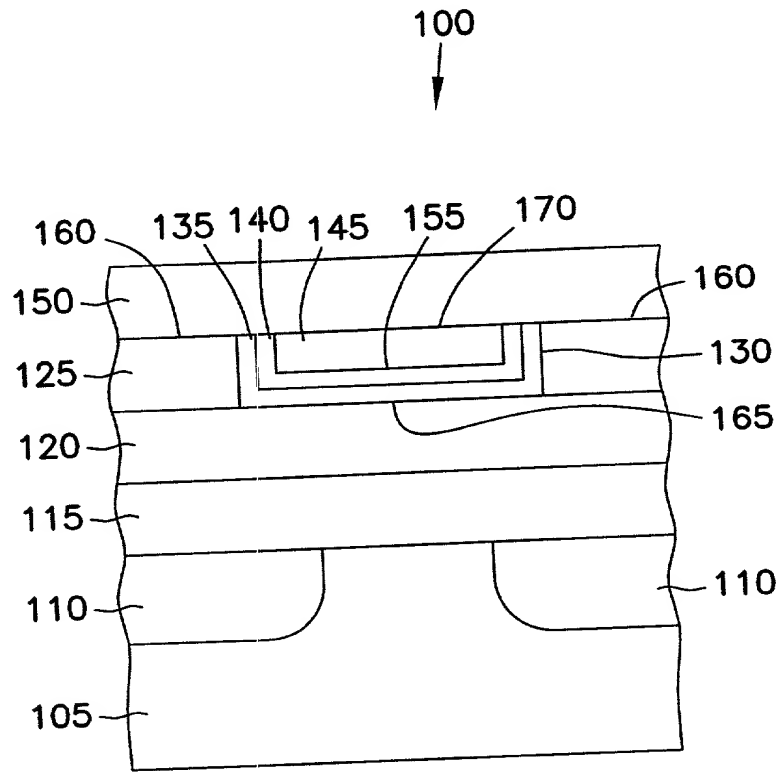


Figure 1

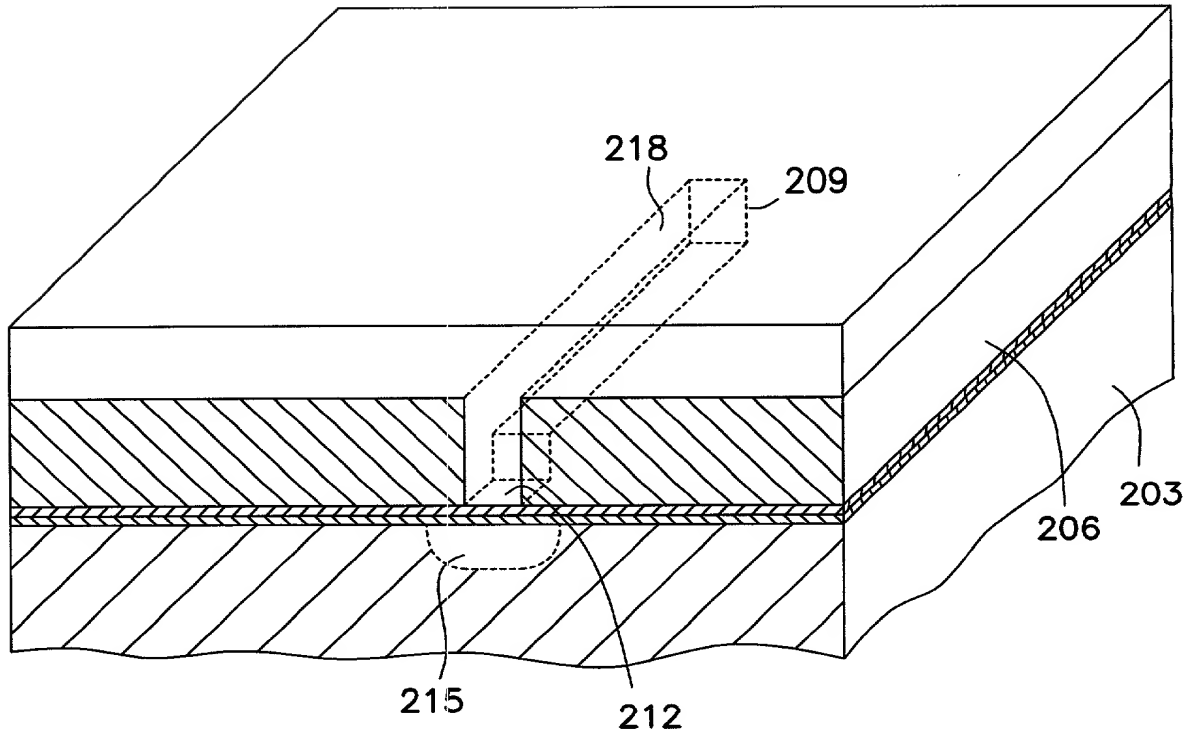


Figure 2A

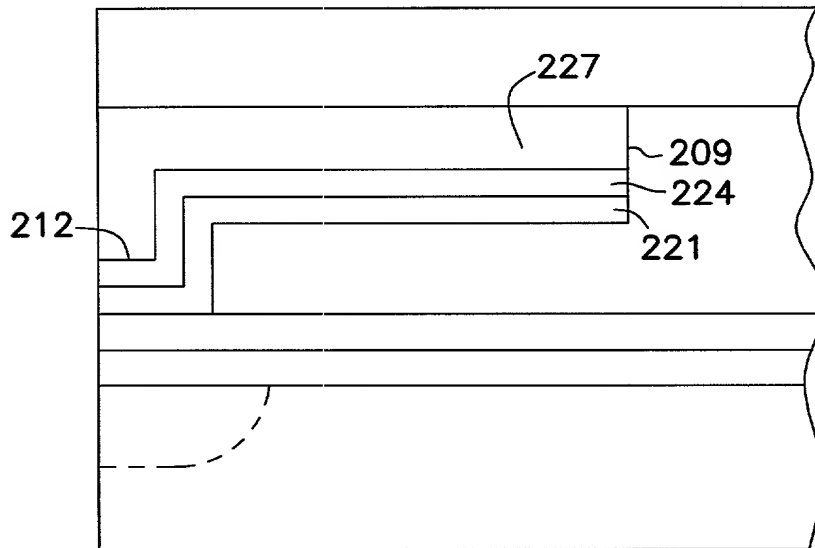


Figure 2B

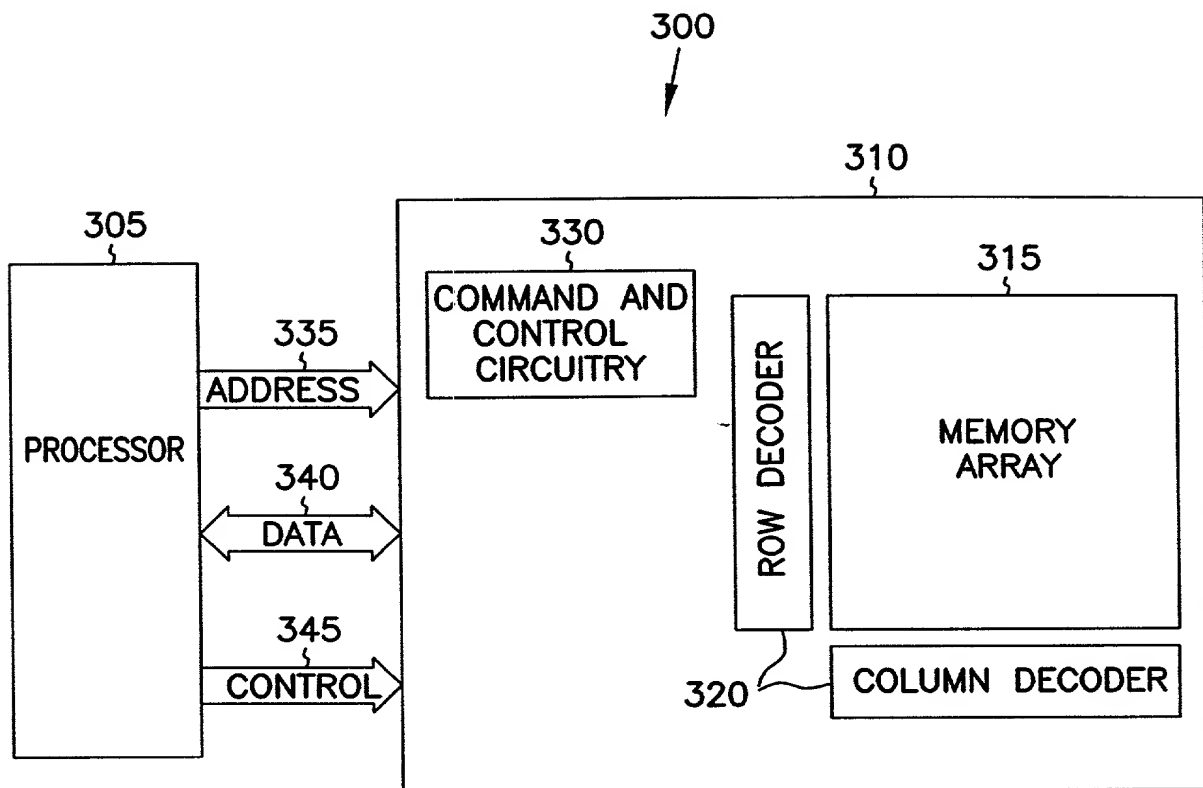


Figure 3

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: CONDUCTIVE STRUCTURES IN INTEGRATED CIRCUITS.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Adams, Matthew W	Reg. No. P-43,459	Forденbacher, Paul J.	Reg. No. 42,546	Maki, Peter C.	Reg. No. 42,832
Anglin, J. Michael	Reg. No. 24,916	Forrest, Bradley A.	Reg. No. 30,837	Mates, Robert E.	Reg. No. 35,271
Arora, Suneel	Reg. No. 42,267	Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. 42,858
Bianchi, Timothy E.	Reg. No. 39,610	Holloway, Sheryl S.	Reg. No. 37,850	Oh, Allen J.	Reg. No. 42,047
Billion, Richard E.	Reg. No. 32,836	Huebsch, Joseph C.	Reg. No. 42,673	Padys, Danny J.	Reg. No. 35,635
Black, David W.	Reg. No. 42,331	Kalis, Janal M.	Reg. No. 37,650	Pappas, Lia M.	Reg. No. 34,095
Brennan, Thomas F.	Reg. No. 35,075	Klima-Silberg, Catherine I.	Reg. No. 40,052	Polglaze, Daniel J.	Reg. No. 39,801
Brooks, Edward J., III	Reg. No. 40,925	Kluth, Daniel J.	Reg. No. 32,146	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Lacy, Rodney L.	Reg. No. 41,136	Sieffert, Kent J.	Reg. No. 41,312
Drake, Eduardo E.	Reg. No. 40,594	Leffert, Thomas W.	Reg. No. 40,697	Slifer, Russell D.	Reg. No. 39,838
Dryja, Michael A.	Reg. No. 39,662	Lemaire, Charles A.	Reg. No. 36,198	Steffey, Charles E.	Reg. No. 25,179
Eliseeva, Maria M.	Reg. No. 43,328	Litman, Mark A.	Reg. No. 26,390	Terry, Kathleen R.	Reg. No. 31,884
Emбетson, Janet E.	Reg. No. 39,665	Lundberg, Steven W.	Reg. No. 30,568	Viksnins, Ann S.	Reg. No. 37,748
Famey, W. Bryan	Reg. No. 32,651	Lynch, Michael L.	Reg. No. 30,871	Woessner, Warren D.	Reg. No. 30,440
Fogg, David N.	Reg. No. 35,138				

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)373-6900

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Paul A. Farrar**
Citizenship: **United States of America** Residence: **So. Burlington, VT**
Post Office Address: 17 Yandow Drive
So. Burlington, VT 05403

Signature: _____ Date: _____
Paul A. Farrar

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
- (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application;
- (2) Each attorney or agent who prepares or prosecutes the application; and
- (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.